LDDP-20-70

Description

LDDP-20-70 is an OEM driver module for integration designed to supply laser diode strings of multiple single emitters in series.
Its unique buck/boost switching topology allows DC/DC operation with load compliance voltage even exceeding the DC input voltage: Standard diode drivers with buck converter require a load voltage for minimum ca. 2 V below the supply input.
LDDP can supply loads from 0 .. 70 V from a DC input between 12 .. 52 V, as long as the input current does not exceed 25 A.
System designers can thus keep using usual e.g. low cost 24 V auxiliary supplies although more and more laser diodes exceed yet the 30 V compliance voltage level.

LDDP-20-70 is fast analog regulated. The up to 99 % highly efficient switching regulation provides pulses or up to 100 % amplitude modulation with typ. 200 µs rise/fall times.
An even faster high speed model (-HS) with typ. rise/fall times <65 µs and analog modulation to >10 kHz is optionally available.

Besides standard industrial and medical use its low current ripple/noise makes it especially suitable for sensitive pumping applications.
The standard model provides differential signal I/Os for all digital and analog signals.

Features

- Output current up to 20 A
- Buck/boost U_{out} = 0 .. 70 V independent of U_{in}
- typ. 200 µs rise/fall time
- Low current ripple/noise <±0.25% pp/0.1% rms
- Efficiency to 99 %
- Especially suitable for fiber laser amplifiers and burn-in systems with multiple single emitter strings

Specifications

Output	0 .. 20 A / 0 .. 70 V *1)
Rise time	typ. 200 µs
Current ripple	typ. <±0.25% (of full scale)
Current programming	0 .. 10 V = 0 .. 20 A (2 A/V)
Prog. accurracy	typ. <±1 % (of set-point within specified range)
Monitoring I/U	0 .. 10 V (I_{mon} 0.5 V/A, U_{mon} 0.1 V/V, real time)
Monitoring accurracy	typ. ±0.5 % (of set-point within specified range)
Protective features/ error output	Monitor starting sequence, soft start, transient protection, OVP, over temperature, over current, protection shut down reaction time <1 µs Fault = high impedance, ok = low imp.
Control interface	Quasi isolated: Interface GND can float max. ±5 V versus negative input terminal, connector JST 16pin S16B-PADSS-1 Digital interface upon request
Efficiency	typ. 97.5 .. 98.5 %
Input	typ. 48 VDC, allowed range 12 .. 52 VDC *2)
Input capacity	1 mF
Environment	-20 °C .. +50 °C (non condensing)
Cooling	Conductively via baseplate, max. power dissipation 25 W
Baseplate temperature	max. +50 °C
DC connectors in/out	Screw terminals M4
Size (LxWxH)	ca. 120 x 75 x 34 mm

1) max. output power up to 1000 W. Higher output power on request.
Specified output voltage range 2 .. 70 V, independent of input voltage (U_{in} 24 .. 52 V DC).
Input current must not exceed 25 A. Specified output range 2 .. 20 A
*2) calibrated standard 24 .. 48 VDC. Operation at 12 VDC (±10%) input possible.
Consult product management for calibration adjustment

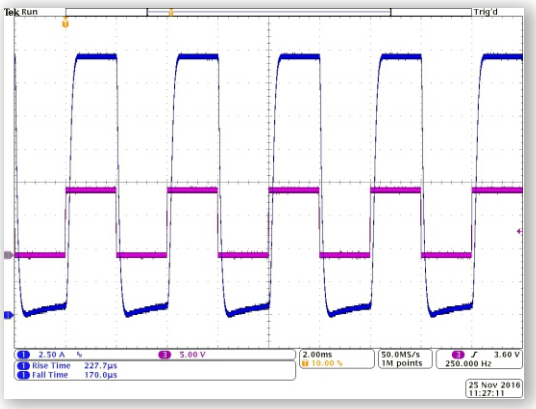

fig. 01

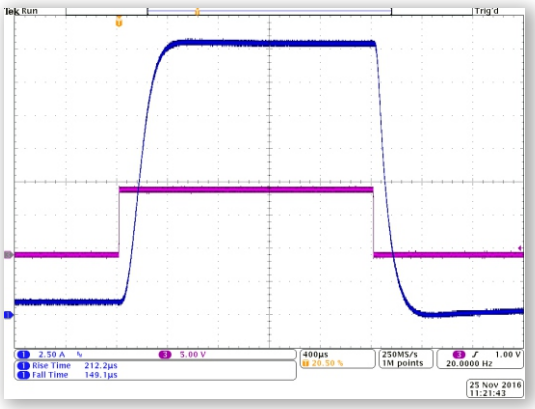

fig. 02

LDDP-20-70-10P-HS

Description

LDDP-20-70 is designed to supply laser diode strings of multiple single emitters in series.
Its unique buck/boost switching topology allows DC/DC operation with load compliance voltage even exceeding the DC input voltage: Standard diode drivers with buck converter require a load voltage for minimum ca. 2 V below the supply input.
LDDP can supply loads from 0 .. 70 V from a DC input between 12 .. 52 V, as long as the input current does not exceed 25 A.
System designers can thus keep using usual low cost 24 V auxiliary supplies although more and more laser diodes exceed yet the 30 V compliance voltage level.

The high speed model LDDP-20-70-HS is fast analog regulated. The up to 97 % highly efficient switching regulation provides fast pulses to 2 kHz or to 5 kHz (-3 dB) analog amplitude modulation with typ. 50 .. 65 µs rise/fall times. At lower modulation depth even faster modulation to >10 kHz is possible.

Besides standard industrial and medical use for direct diode applications its low current ripple/noise makes it especially suitable for sensitive pumping applications.
The standard model provides differential signal I/Os for all digital and analog signals.
A 10pin interface (-10P) provides common GND w/ differential setpoint input.

Features

- Output current up to 20 A
- Buck/boost U_{out} = 0 .. 70 V independent of U_{in}
- typ. 50 .. 65 µs rise time
- Very low current ripple/noise typ. 0.15 % p-p
- Efficiency to 97 %
- Especially suitable for fiber laser amplifiers and direct diode applications with multi single emitter strings

Specifications

Output	0 .. 20 A / 0 .. 70 V *1)
Rise time	< 65 µs
Current ripple (peak-peak)	typ. ±0.15% p-p (buck) / ±0.35 % p-p (boost)
Current programming	0 .. 10 V = 0 .. 20 A (2 A/V)
Prog. accurracy	typ. <±1 % (of set-point within specified range)
Monitoring I/U	0 .. 10 V (I_{mon} 0.5 V/A, U_{mon} 0.1 V/V, real time)
Monitoring accurracy	typ. ±0.5 % (of set-point within specified range)
Protective features/ error output	Monitor starting sequence, soft start, transient protection, OVP, over temperature, over current, protection shut down reaction time <1 µs Fault = high impedance, ok = low imp.
Control interface	Quasi isolated: Interface GND can float max. ±5 V versus negative input terminal, connector JST 16pin S16B-PADSS-1 Digital interface upon request
Efficiency	typ. 95 .. 97 %
Input	typ. 48 VDC, allowed range 12 .. 52 VDC *2)
Input capacity	1 mF
Environment	-20 °C .. +50 °C (non condensing)
Cooling	Conductively via baseplate, max. power dissipation 25 W
Baseplate temperature	max. +50 °C
DC connectors in/out	Screw terminals M4
Size (LxWxH)	ca. 120 x 75 x 34 mm

1) max. output power up to 800 W. Higher output power on request.
Specified output voltage range 2 .. 70 V, independent of input voltage (U_{in} 24 .. 52 V DC).
Input current must not exceed 25 A. Specified output range 2 .. 20 A
*2) calibrated standard 24 .. 48 VDC. Operation at 12 VDC (±10%) input possible.
Consult product management for calibration adjustment

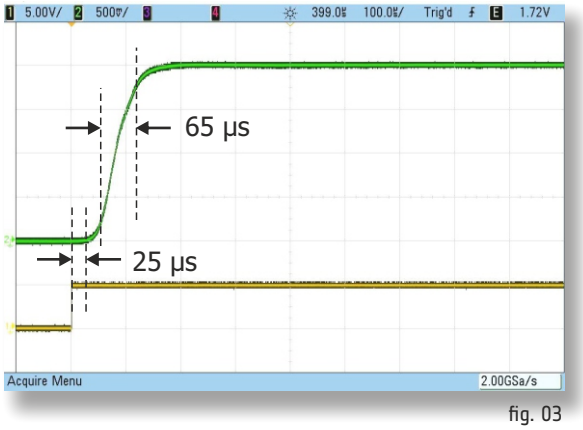

fig. 03

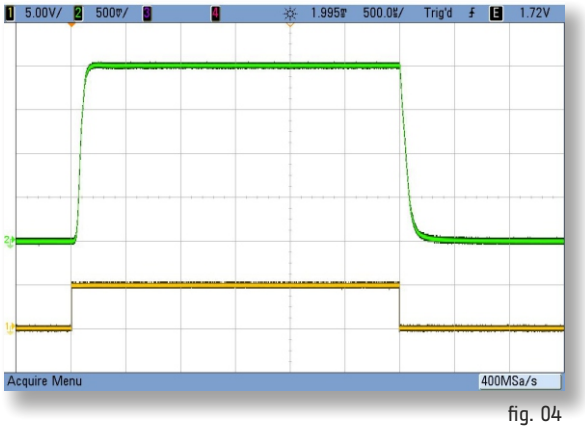

fig. 04

Operation / starting sequence:

- Mount the driver to a proper heat sink. Max. power dissipation <=20 W, typical efficiency 97 .. 98% –> refer to fig. 16

- Connect supply, load cables and control signals -> refer to fig. 7 and table below (fig. 05)
  Load cables should always be kept as short as possible, e.g. 1 m cable length is considered yet to be long.
  Long cables are possible to be used, but not recommended due to higher inductance/reduced rise/fall time performance.
  Use twisted pair or similar low inductance cables to connect your diode load.

- Starting sequence (recommended for standard operation / mandatory for pulsed operation):
  1. Close interlock and apply supply power to power input (LED 1 = green)
  2a. Enable driver (LED 2 = amber).
  2b. Apply setpoint: Output current equals setpoint programming voltage by 2 A/V
  2c. Set pulse pin HIGH

  Subitems a/b/c under point 2 can be interchange without provoking an error.
  Setting enable HIGH before the interlock is closed will latch the driver disabled.
  Opening the interlock during enable = Fault (LED3 [red] = ON). Toggle driver Enable with interlock closed to unlatch.
  The properly enabled driver will output current to the connected load, if I-setpoint is > 0 V.
  A small residual current in the mA regime can also be present, if in enabled status I-setpoint = 0. To eliminate any current flow disable driver.
  HIGH signal to pulse input may be applied any time and does not affect the starting sequence.
  Enabling driver with pulse pin HIGH will lead to a softstart current slope of ca. 10 ms.

  Intrinsic load break protection: In case of a loose load contact during current operation above 500 mA shuts down driver very fast and shorts the output crowbar.
  Efficiency will be highest, if driver operates in buck mode (ca. U_{in} > U_{out}+4V) and buck-boost mode (U_{in} = ca. U_{out}). Efficiency will decrease by typ. 0.5..1% in boost mode, at lower input voltage or at high input current. (refer to fig. 16)

  Altering DC input voltage might affect driver output linearity. Specifications not for dynamic, but for fixed input voltage only during operation.

Maximum pulse performance by pin 5/13 and analog modulation speed is limited only by the intrinsic regulation speed (rise/fall time) and may reach up to 2 kHz or higher at reduced modulation depth.

Interface logic

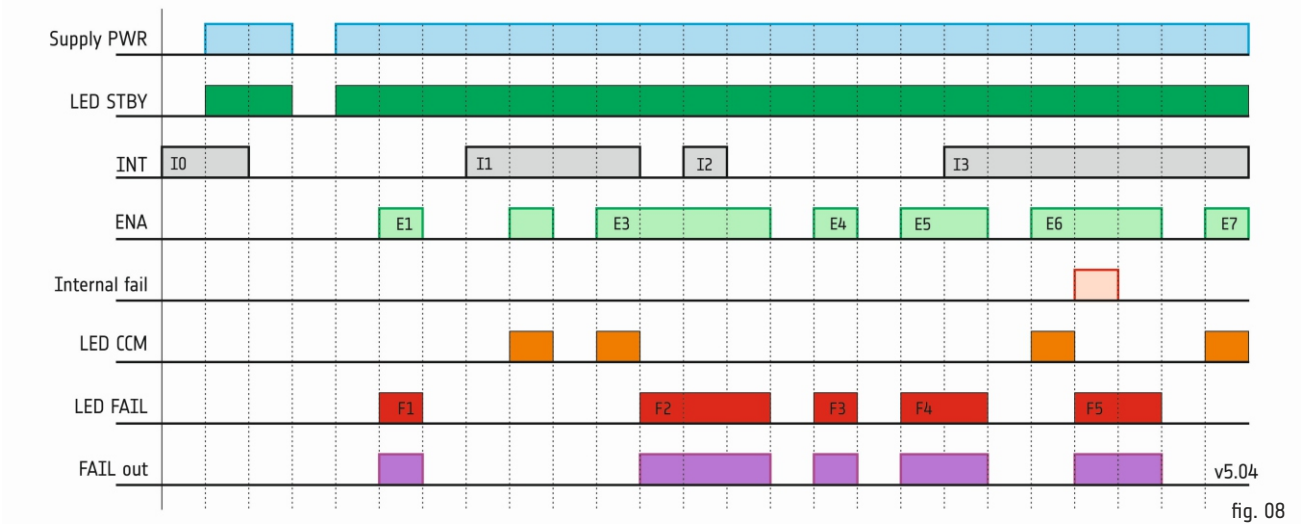

fig. 08

Interface: Standard 16pin (socket # S16B-PADSS-1)

Pin		Signal	Comments
1		I-setpoint +I	0-10 V analog setpoint/programming input
2		I-setpoint RTN	setpoint/programming input RTN
3		GND	analog GND
4		ENA	optically isolated Enable input, +5 V..24 V vs. ENA_RTN enables driver
5		PULSE	+5 V..24 V vs. pin 13/PULSE_RTN switches output ON
6		INTERLOCK	a) input +5 .. 24 V vs. pin 12 (INT_RTN) **OR** b) make floating short to pin 15/INTERLOCK source
7		MON-U	Voltage monitor output, 0.1 V/V
8		MON-I	Current monitor output, 0.5 V/A

Pin		Signal	Comments
9		FAIL feedback	Optically idolated error signal, contact NC vs. GND: In case or error vs. FAIL_RTN opened (max. 80 V/3 mA)
10		GND	analog GND
11		ENA_RTN	see pin 4, enable return pin
12		INTERLOCK RTN	per standard connected via 0R0 to analog GND (note also remark on pin 15 regarding GND reference)
13		PULSE_RTN	see pin 5, pulse return pin
14		FAIL_RTN	see pin 9, failure return pin
15		+5V aux / INTERLOCK source	aux +5 V/max. 10 mA, imp. 100 Ω, user must protect against over current. Usable as Interlock source to set pin 6 high, if pin 12 has contact to analog GND
16		GND	analog GND

fig. 05

Model options

High speed option -HS: For rise/fall times ca. 65 µs and analog modulation to ca. 10 kHz
10pin option -10P: 10pin instead of 16pin interface for common analog and digital GND. Only I-set +/- differential

Pin		Signal	Comments
1		I-setpoint +I	0-10 V (differential) analog setpoint/programming input
2		I-setpoint RTN	differential setpoint/programming input RTN vs. pin1
3		GND	common analog & digital GND
4		ENA	Enable input (slow): +5 V..24 V enables driver
5		PULSE	Pulse input (fast): +5 V..24 V switches output ON
6		INTERLOCK	Input +5 .. 24 V closes interlock
7		MON-U	Voltage monitor output, 0.1 V/V
8		MON-I	Current monitor output, 0.5 V/A

Pin		Signal	Comments
9		FAIL feedback	Optically isolated error signal, contact NC vs. GND: In case or error opened (max. 80 V/3 mA)
10		GND	common analog & digital GND

pins 11 to 16 void due to 10pin option -10P

-10P socket # S10B-PADSS-1

fig. 06

Interface equivalent circuit

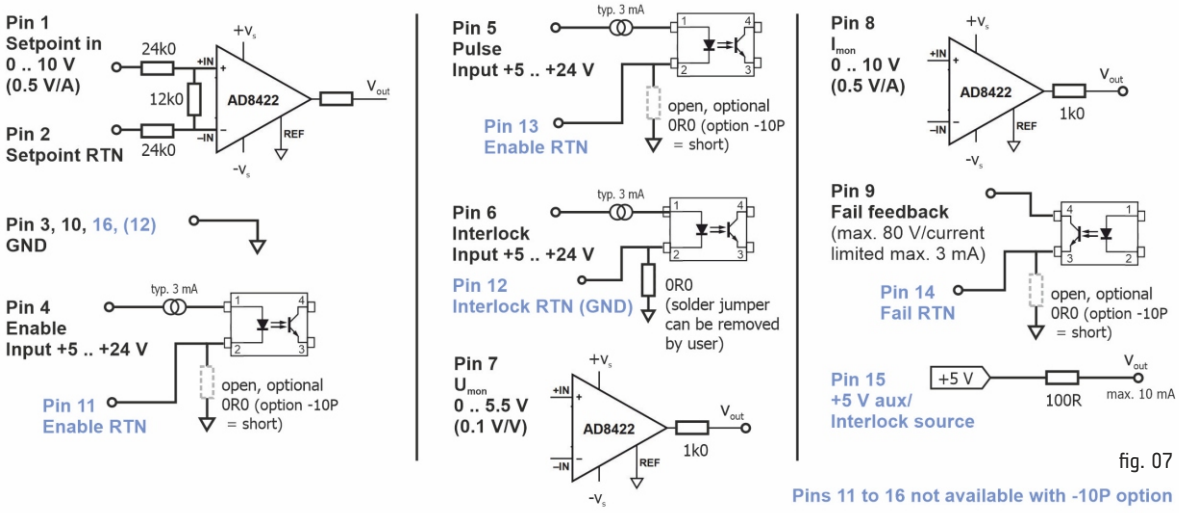

fig. 07

Remarks:

- Optionally available for easiest integration: 1 meter connection cable w/ above defined wire color code to meet JST S16B-PADSS-1.
- Error output pins are open/high impedance in power-off status.
- Pin 15 ("Aux / Interlock source") must be used only vs. proper LDDP GND pins 3/10/16 (12) and/or closed vs. pin 6 by a floating contact/switch. Do not use other external GND potential!
- I-setpoint input is high impedance (60 kOhm). To avoid external noise coupling in, grounding pin 2 (I-setpoint_RTN) to PE may be required.
- Attention: Floating diode load required at main output: Interface GND is limited to float ±5 V only in respect to negative output/load connector.

PCB functional description and connectors:

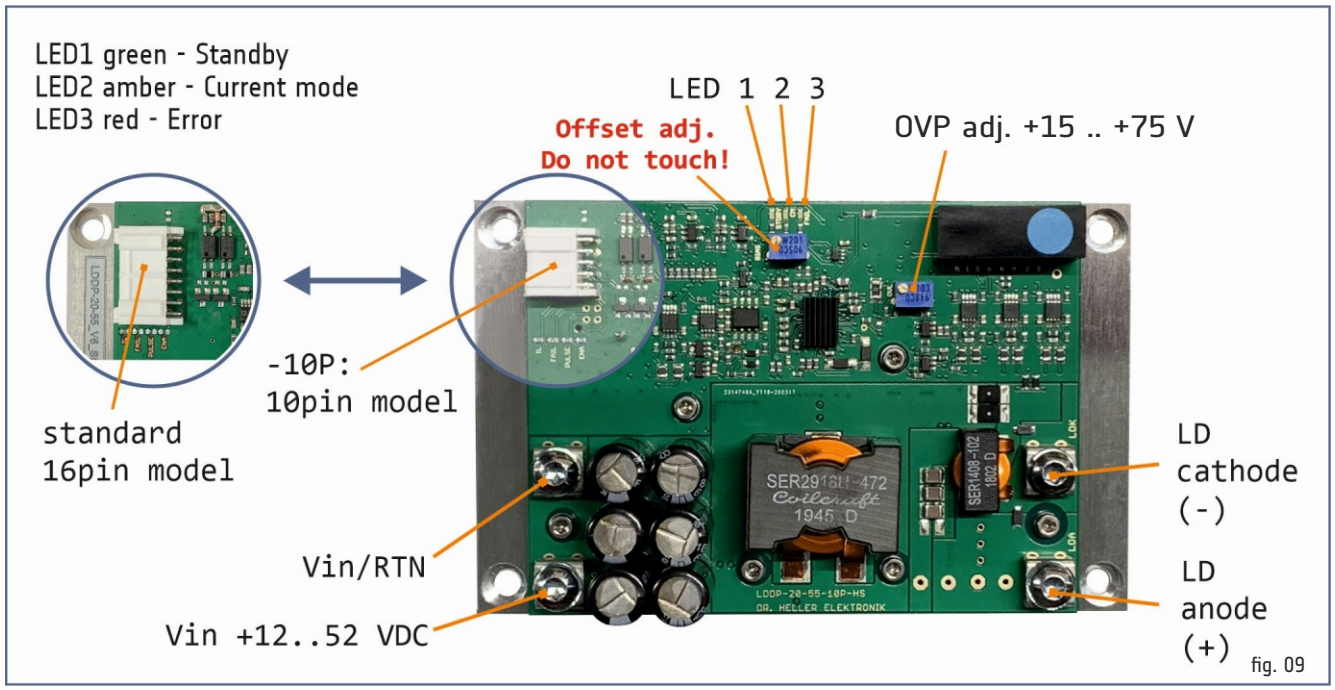

fig. 09

Mechanical drawing:

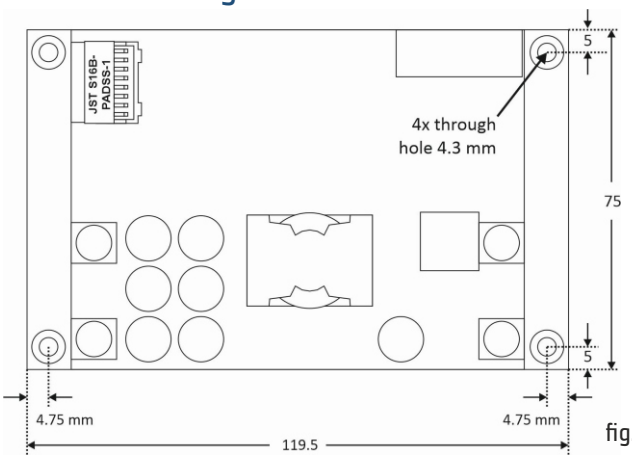

fig. 10

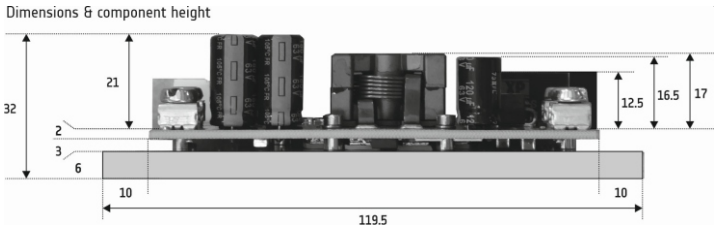

fig. 11

Remarks:

Please note that LDDP-20-70 is a buck/boost converter with an extremely wide in- & output parameter range. Whilst the standard models are suitable for about 95% of standard applications within its parameter range, any parameter of LDDP can become custom optimized for a certain application.
Adapted regulation speed, even lower ripple, maximum and minimum operating voltage and current, higher peak power up to >1 kW – for any parameter we are open to optimize the product according to the user specific needs.

➔ Please ask us!

Pulsed operation and analog modulation:

For fast pulsed operation the output current set-point must be set before output is activated by pulse pin (5/13).
Pulsed operation and analog modulation can be performed up to ca. 2 kHz at full scale. Analog modulation at lower modulation depth will be higher

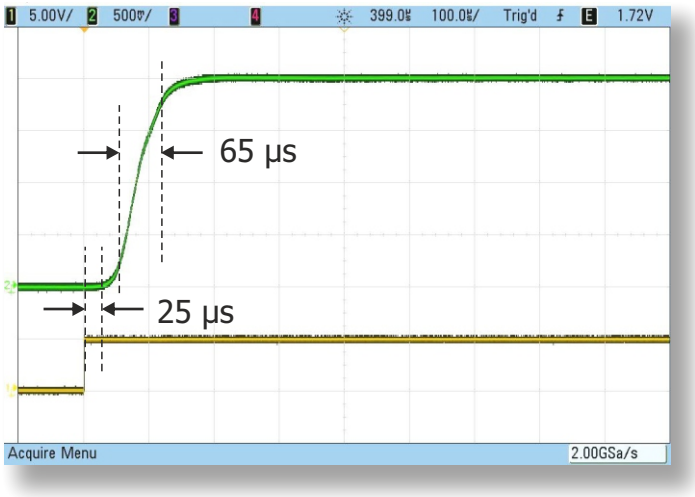

fig. 12

Scaling 100 µs/div, vertical 5 A/div
Current step 0 -> 20 A, Rising edge (10..90%) ca. 100 µs

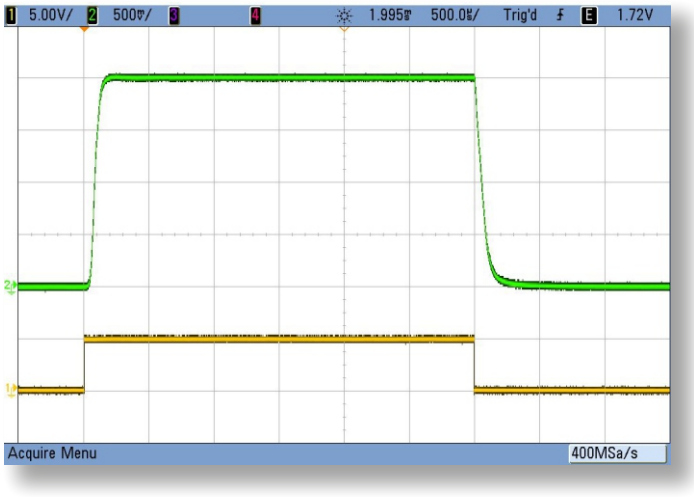

fig. 13

Scaling 500 µs/div, vertical 5 A/div
Current step 0 -> 20 A, pulse width 3 ms

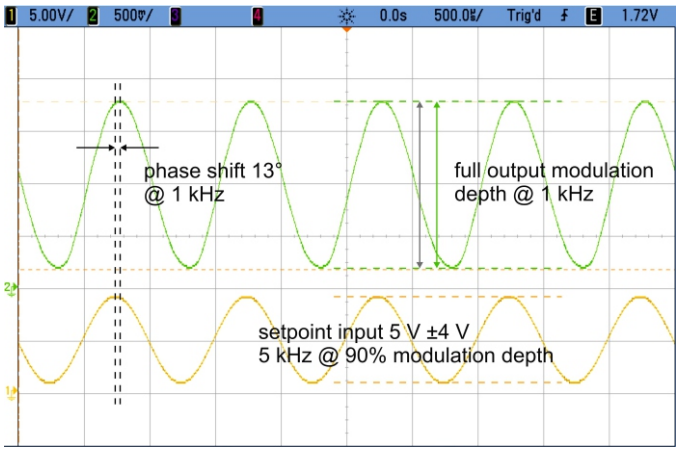

fig. 14

Scaling 500 µs/div, vertical green 5 A/div, amber 5 V/div,
Analog 90 % setpoint modulation @1 kHz:
No perceptible attenuation

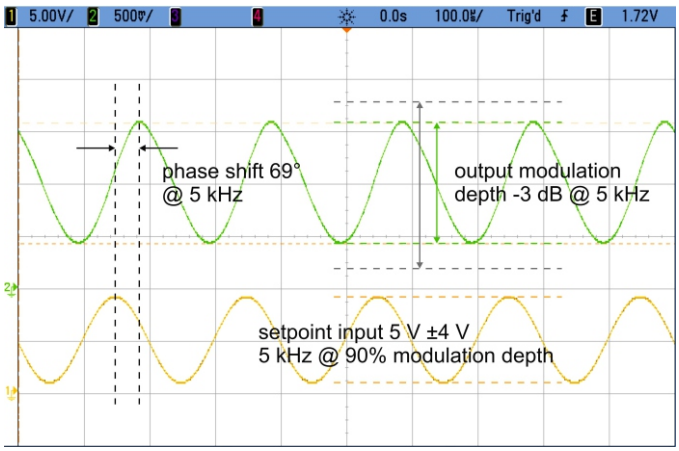

fig. 15

Scaling 100 µs/div, vertical green 5 A/div, amber 5 V/div,
Analog 90 % setpoint modulation @5 kHz:
Attenuation ca. -3 dB

Efficiency / cooling:

The efficiency of LDDP-20-70 is extraordinarily high. Depending on the operating mode efficiency is between ca. 92 .. 99%.
Typical efficiency values as follows:

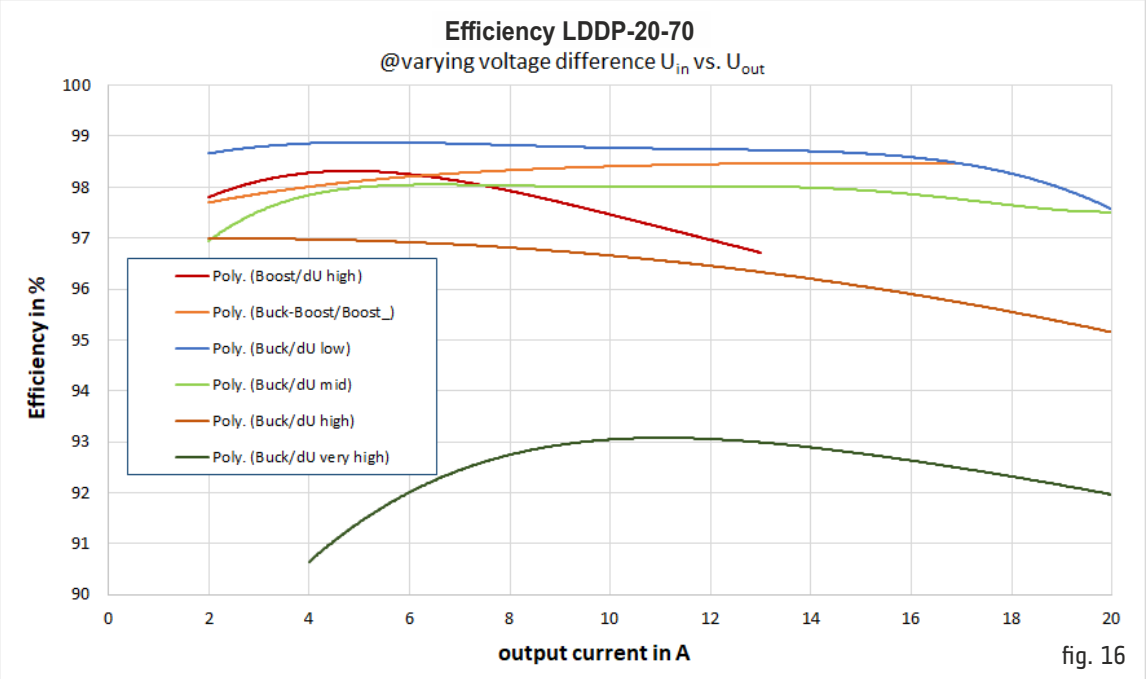

fig. 16

1. Buck mode @lowest output (dU = U_{in} – U_{out} = very high): U_{in} = 48 VDC and $U_{compliance}$ = ca. 2 .. 10 V, η_{typ} = 92 .. 93%
2. Buck mode @low output voltage (dU = U_{in} – U_{out} = high): U_{in} = 48 VDC and $U_{compliance}$ = ca. 10 .. 20 V, η_{typ} = 96 .. 97%
3. Buck mode @mid output voltage (dU = U_{in} – U_{out} = mid): U_{in} = 48 VDC and $U_{compliance}$ = ca. 20 .. 35 V, η_{typ} = 98%
4. Buck mode @high output voltage (dU = U_{in} – U_{out} = low): U_{in} = 48 VDC and $U_{compliance}$ = ca. 35 .. 45 V, η_{typ} = 98 .. 99%
5. Buck-boost mode: (U_{in} = ca. U_{out}): U_{in} = 48 VDC and $U_{compliance}$ = ca. 45 .. 52 V, η_{typ} = 98%
6. Boost mode: (U_{in} < U_{out}): U_{in} = 24 VDC and $U_{compliance}$ = ca. 25 .. 37 V, η_{typ} = 97 .. 98%

During tested output power of up to 1 kW by the driver´s dissipated heat always remained <= 25 W.
Anyway, if continuous or pulsed output power above 1000 W peak (or 800 W peak for -HS model) is required, please contact our product management.
Highspeed model LDDP-20-70-HS has an efficiency approx. 1 to 2 % lower than the standard low speed model.

Optional accessory

fig. 17

Interface connector cable w/ color code according to fig. 05 (16-pin, article # HD0993).
or fig. 06 (10-pin, article # HD0987)

fig. 18

1550-LDDC handheld controller & 1550-LDDC-OEM controller: For manual or remote control (USB/RS232), CW to pulsed/burst operation. For additional synchronization purpose, delay operation, etc. please ask for 1650-LSC.
-> **Adaptor cable available** for direct connection of 1550/1650 w/ LDDP

Operation / starting sequence:

- Mount the driver to a proper heat sink. Max. power dissipation <=20 W, typical efficiency 97 .. 98% –> refer to fig. 16

- Connect supply, load cables and control signals -> refer to fig. 7 and table below (fig. 05)
  Load cables should always be kept as short as possible, e.g. 1 m cable length is considered yet to be long.
  Long cables are possible to be used, but not recommended due to higher inductance/reduced rise/fall time performance.
  Use twisted pair or similar low inductance cables to connect your diode load.

- Starting sequence (recommended for standard operation / mandatory for pulsed operation):
  1. Close interlock and apply supply power to power input (LED 1 = green)
  2a. Enable driver (LED 2 = amber).
  2b. Apply setpoint: Output current equals setpoint programming voltage by 2 A/V
  2c. Set pulse pin HIGH

  Subitems a/b/c under point 2 can be interchange without provoking an error.
  Setting enable HIGH before the interlock is closed will latch the driver disabled.
  Opening the interlock during enable = Fault (LED3 [red] = ON). Toggle driver Enable with interlock closed to unlatch.
  The properly enabled driver will output current to the connected load, if I-setpoint is > 0 V.
  A small residual current in the mA regime can also be present, if in enabled status I-setpoint = 0. To eliminate any current flow disable driver.
  HIGH signal to pulse input may be applied any time and does not affect the starting sequence.
  Enabling driver with pulse pin HIGH will lead to a softstart current slope of ca. 10 ms.

  Intrinsic load break protection: In case of a loose load contact during current operation above 500 mA shuts down driver very fast and shorts the output crowbar.
  Efficiency will be highest, if driver operates in buck mode (ca. U_{in} > U_{out}+4V) and buck-boost mode (U_{in} = ca. U_{out}). Efficiency will decrease by typ. 0.5..1% in boost mode, at lower input voltage or at high input current. (refer to fig. 16)

  Altering DC input voltage might affect driver output linearity. Specifications not for dynamic, but for fixed input voltage only during operation.

Maximum pulse performance by pin 5/13 and analog modulation speed is limited only by the intrinsic regulation speed (rise/fall time) and may reach up to 2 kHz or higher at reduced modulation depth.

Interface: Standard 16pin (socket # S16B-PADSS-1)

Pin	Signal	Comments
1	I-setpoint +I	0-10 V analog setpoint/programming input
2	I-setpoint RTN	setpoint/programming input RTN
3	GND	analog GND
4	ENA	optically isolated Enable input, +5 V..24 V vs. ENA_RTN enables driver
5	PULSE	+5 V..24 V vs. pin 13/PULSE_RTN switches output ON
6	INTERLOCK	a) input +5 .. 24 V vs. pin 12 (INT_RTN) **OR** b) make floating short to pin 15/INTERLOCK source
7	MON-U	Voltage monitor output, 0.1 V/V
8	MON-I	Current monitor output, 0.5 V/A

Pin	Signal	Comments
9	FAIL feedback	Optically idolated error signal, contact NC vs. GND: In case or error vs. FAIL_RTN opened (max. 80 V/3 mA)
10	GND	analog GND
11	ENA_RTN	see pin 4, enable return pin
12	INTERLOCK RTN	per standard connected via 0R0 to analog GND (note also remark on pin 15 regarding GND reference)
13	PULSE_RTN	see pin 5, pulse return pin
14	FAIL_RTN	see pin 9, failure return pin
15	+5V aux / INTERLOCK source	aux +5 V/max. 10 mA, imp. 100 Ω, user must protect against over current. Usable as Interlock source to set pin 6 high, if pin 12 has contact to analog GND
16	GND	analog GND

fig. 05

-> see next page, fig. 06 for -10P interface configuration

Remarks:
- Optionally available for easiest integration: 1 meter connection cable w/ above defined wire color code to meet JST S16B-PADSS-1.
- Error output pins are open/high impedance in power-off status.
- Pin 15 ("Aux / Interlock source") must be used only vs. proper LDDP GND pins 3/10/16 (12) and/or closed vs. pin 6 by a floating contact/switch.
  Do not use other external GND potential!
- I-setpoint input is high impedance (60 kOhm). To avoid external noise coupling in, grounding pin 2 (I-setpoint_RTN) to PE may be required.
- Attention: Floating diode load required at main output: Interface GND is limited to float ±5 V only in respect to negative output/load connector.

Model options

High speed option -HS: For rise/fall times ca. 65 µs and analog modulation to ca. 10 kHz
10pin option -10P: 10pin instead of 16pin interface for common analog and digital GND. Only I-set +/- differential

Pin		Signal	Comments
1		I-setpoint +I	0-10 V (differential) analog setpoint/programming input
2		I-setpoint RTN	differential setpoint/programming input RTN vs. pin1
3		GND	common analog & digital GND
4		ENA	Enable input (slow): +5 V..24 V enables driver
5		PULSE	Pulse input (fast): +5 V..24 V switches output ON
6		INTERLOCK	Input +5 .. 24 V closes interlock
7		MON-U	Voltage monitor output, 0.1 V/V
8		MON-I	Current monitor output, 0.5 V/A

Pin		Signal	Comments
9		FAIL feedback	Optically isolated error signal, contact NC vs. GND: In case or error opened (max. 80 V/3 mA)
10		GND	common analog & digital GND

pins 11 to 16 void due to 10pin option -10P

-10P socket # S10B-PADSS-1

fig. 06

Interface – equivalent circuit

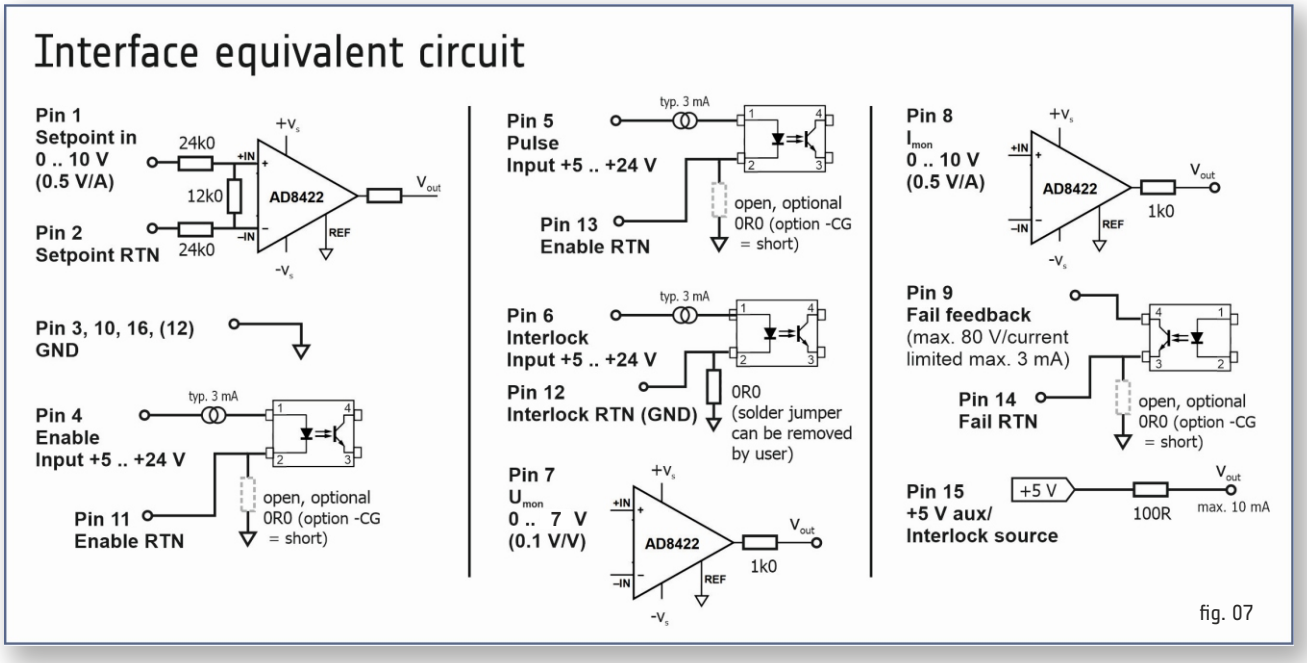

fig. 07

Interface logic

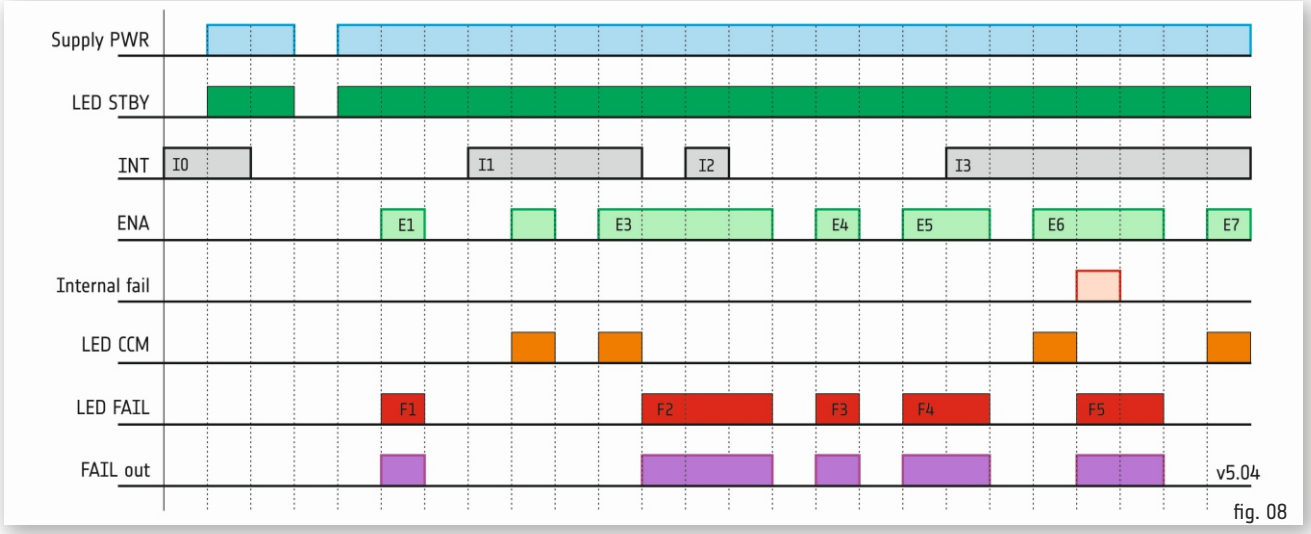

fig. 08